CLAIMS

What is claimed is:

1. A non-volatile memory cell structure, said structure comprising:

an N-type well region in a substrate, a channel region between a P-type source region and a P-type drain region, wherein the conductivity type of said P-type is opposite to said N-type;

a first insulator layer on the surface of said N-type well region;

a floating gate overlying said first insulator layer;

a second insulator layer on said floating gate; and

a control gate on said second insulator layer, wherein said non-volatile memory cell is erased by applying an erase voltage to said P-type drain region, applying a supply voltage to said control gate, and said erase voltage applied to said N-type well region.

2. The structure according to claim 1, wherein said erase voltage between about 12 volts.

3. The structure according to claim 1, further comprising a source line coupled to said P-type source region, said source line exhibits floating.

4. The structure according to claim 3, wherein said source line is divided by an isolation structure along a bit line direction.

5. A semiconductor memory cell structure, said structure comprising:

an N-type well region in a substrate, a channel region between a P-type drain region and a P-type source region, wherein the conductivity type of said N-type is opposite to said P-type;

a insulator layer overlying said N-type well region; and

a gate transistor on said insulator layer, said gate transistor comprises a control gate coupled to a word line, said P-type drain region coupled to a bit line, wherein said cell is erased by applying an erase voltage between about 12 volts to said P-type drain region, and applying a supply voltage to said control gate.

6. The structure according to claim 5, wherein said P-type source region coupled to a source line.

7. The structure according to claim 6, wherein said source line is divided along a bit direction by using an isolation structure.

8. The structure according to claim 5, wherein a supply voltage applied to said N-type well region is erase voltage.

9. The structure according to claim 5, wherein said cell is programmed by applying a negative supply voltage between 6-10 to said P-type drain region to induce hot electron, and a negative threshold voltage is of about 2 volts applied to said word line.

10. A method for erasing non-volatile memory cell having a P-type substrate and an N-type well region therein, a channel region between a P-type drain region and a P-type source region, said method comprising the steps of:

applying an erase voltage to said P-type drain region to cause tunneling of electrons from a floating to said N-type well region and to said N-type well region, wherein said P-type drain region coupled to a bit line;

applying a supply voltage to a control gate, wherein said control gate coupled to a word line; and

grounding said word line of unselected cell and said bit line of unselected cell to cause the P-type drain region as an inhibit switch.

11. The method according to claim 10, wherein said erase voltage is of about 12 volts.